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| 10/528,925 | 09/23/2005 | Steffen Heinz | 00265P0003 WO US | 8774 |

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| EXAMINER | |
|---|---|
| HERNANDEZ, WILLIAM | |

| ART UNIT | PAPER NUMBER |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/528,925 | HEINZ ET AL. | |
| | Examiner | Art Unit | |
| | William Hernandez | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *10-18* is/are pending in the application.

4a) Of the above claim(s) *16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-15,17 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 March 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

Applicant's amendment has been received and entered in the case. The amendments and arguments presented therein overcome the informality objections and indefiniteness rejections, and therefore, these are withdrawn. However, the amendments and arguments do not overcome the prior art rejections, and therefore, these are maintained.

### *Drawings*

1. The replacement drawings were received on 3/14/07. These drawings are acceptable.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 10, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanzawa et al. (USP 6,600,679 B2) in view of Arnold (USP 3,980,897).

Tanzawa's Fig. 6 shows a circuit arrangement for bridging high voltages using a switching signal, comprising:

a voltage transmitter with first (Vh) and second (Vl) terminals for a low voltage;

a voltage receiver with third (VH) and fourth (VH) terminals for a higher voltage relative to the low voltage between the first and second terminals, wherein the voltage transmitter and the voltage receiver each comprise a first inverter circuit (I3 and I2, respectively) and a second inverter circuit (I4 and I1, respectively),

wherein the inverter circuits of the voltage transmitter are connected between the first and second terminals and the inverter circuits of the voltage receiver are connected between the third and fourth terminals (clearly shown),

wherein an output of the first inverter circuit of the voltage transmitter is connected via a first capacitor (C1) as a high voltage capacitor with an input of the second inverter circuit of the voltage receiver and an output of the first inverter circuit of the voltage receiver, and an output of the second inverter circuit of the voltage transmitter is connected via a second capacitor (C2) as a high voltage capacitor with an input of the first inverter circuit of the voltage receiver and an output of the second inverter circuit of the voltage receiver,

wherein the inputs of the first inverter circuit and the second inverter circuit, respectively, of the voltage transmitter are a non-inverted and an inverted input (ND3 is the complement of IN), and wherein the outputs of the first inverter circuit and the second inverter circuit, respectively, of the voltage receiver represent output nodes (ND1 and ND2),

wherein the circuit arrangement for bridging high voltage with a switching signal is realized as an integrated semi-conductor circuit made with semi-conductor processes

(see title) with high voltage capacitors (C1 and C2 must be high voltage capacitors if they are to accept voltages from the high-voltage inverters I1 and I2).

Tanzawa does not show the inverter circuits implemented as CMOS circuits as called for in claim 10. However, as taught by Arnold, it is old and well known in the art that CMOS inverters and CMOS circuits in general benefit from low power dissipation (col. 1: 29-35). Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to implement the inverters of Tanzawa's level shifter as CMOS circuits for the purpose of lowering power consumption.

As per claim 14, Tanzawa discloses CMOS level circuits (e.g., Fig. 8) for a semiconductor memory device (see title) whose inverters are all CMOS inverters (i.e., complementary transistors connected in series).

As per claim 15, this claim is merely the functionality of the circuit having structure recited in claim 10. Since Tanzawa teaches the structure, the function of the circuit is inherently disclosed.

4. Claims 11-13, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanzawa.

Tanzawa discloses the invention set forth in claim 10 but does not show additional inverters coupled to the inputs of the inverter circuits of the voltage transmitter as called for in claims 11 and 13. However, it is old and well known in the art that adding inverters to the input can be used to control the delay of the circuit. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to couple a third inverter in series with the first voltage transmitter inverter and a

sixth and seventh inverter in series with the second voltage transmitter inverter for the purpose of controlling the circuit's delay for a particular application.

Tanzawa discloses the invention set forth in claim 10 but does not show additional inverters coupled to the outputs of the inverter circuits of the voltage receiver as called for in claim 12. However, it is old and well known in the art that adding an inverter to the output can help in driving the output signal. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to couple a fourth inverter and sixth inverter to the outputs of the voltage receiver for the purpose of providing gain to the output signal.

Tanzawa discloses the invention set forth in claim 10 but does not show the circuit arrangement packaged as an integrated semi-conductor as called for in claims 17 and 18. However, it is old and well known in the art that integrating circuits on a semi-conductor chip has numerous advantages. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to realize Tanzawa's level shifter as an integrated semi-conductor circuit for the purpose of smaller size and lower cost.

### *Response to Arguments*

5. Applicant's arguments filed 3/14/07 have been fully considered but they are not persuasive.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies

(i.e., the digital signal being made available with common voltage levels between approximately 3V to 15V via a potential differential up to several hundred volts to another voltage level) are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Regarding the Tanzawa reference, Applicant argues that Tanzawa does not suggest that the layers are alternatingly connected. This limitation is not required by the claim. Claim 1 reads:

*"the circuit arrangement ... is realized as an integrated semi-conductor circuit ... **or** a stack of layers with alternating layers" [emphasis added].*

As such, only one of the two limitations is required and as clearly seen by Tanzawa's title, the level shifter circuit of Tanzawa meets the limitation wherein the circuit is realized as an integrated semi-conductor circuit.

In summary, claims 10-15, 17 and 18 remain within the scope of the prior art and therefore, no references are withdrawn.

## *Conclusion*

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Hernandez whose telephone number is (571) 272-8979. The examiner can normally be reached on Mon.-Fri. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

WH

TUAN T. LAM
PRIMARY EXAMINER